THAT WHICH IS CLAIMED IS:

1. Method for optimising the functioning of a watchdog timer (1) of a microprocessor (2) having normal time intervals separating refresh commands of the watchdog timer lying within a range having a minimum time period and a maximum time period, the method comprising the steps of:

- receiving refresh commands by the watchdog timer,
- generating a microcontroller reset command by the watchdog timer when the time interval separating successively received refresh commands does not lie within said range, the generation of the reset command comprising:
  - launch of a reset countdown
  - generation of the reset command on timeout of the reset countdown;

the method being characterized in that it also comprises the steps of:

- on each receipt of a refresh command by the watchdog timer, launch of a refresh countdown,
- if the refresh countdown has not timed out at the time of receiving a refresh command, a refresh command does not restart the reset countdown.

2. Method for optimising the functioning of a watchdog timer (1) of a microcontroller (2) according to claim 1, characterized in that:

- the method comprises the steps of:
  - launch of the reset countdown,
  - on receipt of a refresh command by the watchdog timer, launch of the refresh countdown,

- restart of the reset countdown on expiry of the refresh countdown,
- generation of a reset command on expiry of the reset countdown,

also characterized in that the duration of the reset countdown is equal to the maximum time period of said range, the duration of the refresh countdown being equal to the minimum time period of said range.

3. Functioning method according to claim 1, characterized in that it comprises the steps of:

- on receipt of a refresh command by the watchdog timer:
  - if the refresh countdown has timed out, launch of the reset countdown,
  - if the refresh countdown has not timed out, continuation of the reset countdown,
  - launch of the refresh countdown
  - generation of a reset command on expiry of the reset countdown

also characterized in that the duration of the reset countdown is equal to the maximum time period of said range, the duration of the refresh countdown being equal to the minimum time period of said range.

4. Method according to claim 3, characterized in that, if the refresh countdown has timed out, the launch of the reset countdown and the launch of the refresh countdown are conducted simultaneously on receipt of a refresh command.

5. Method according to any of claims 2 to 4, characterized in that the reset countdown is synchronized on a frequency divided clock signal.

6. Method according to any of claims 2 to 5, characterized in that the refresh countdown is synchronized on a clock signal.

7. Method according to any of claims 2 to 6, characterized in that it also comprises a programming step to program the duration of the reset countdown.

8. Method according to claim 7, characterized in that the refresh command received by the refresh input of the refresh counter defines the duration of the reset countdown.

9. Method according to claim 8, characterized in that the refresh command is a word of several bits written in the reset counter during a launch step and defining the duration of the reset countdown.

10. Method according to any of claims 2 to 9, characterized in that the reset counter is a counter with several bits and in that the reset command is generated by transition to low status of the high-order bit (6) of the reset counter.

11. Microcontroller watchdog timer (1) characterized in that it is able to apply the method according to any of claims 1 to 10.

12. Microcontroller watchdog timer (1) according to claim 11, characterized in that it comprises:

- a reset counter (3)

comprising:

- a refresh input (11), and
- a reset output (12), and

designed to:

- launch a reset countdown on receipt of a refresh command on its refresh input (11)
- apply a reset command to reset output (12) when the reset countdown times out;
- a refresh counter (6) connected to refresh input (11) of the reset counter (3), having a refresh input (9), and designed to:
  - launch a refresh countdown on each receipt of a refresh command on its refresh input (9);
  - only to apply a refresh command to refresh input (11) of the reset counter on expiry of the refresh countdown.

13. Watchdog timer according to claim 11, characterized in that it comprises:

- a reset counter (3),

comprising:

- a refresh input (11), and
- a reset output (12), and

designed to:

- launch a reset countdown on receipt of a refresh command on its refresh input (11),
- apply a reset command to reset output (12) on expiry of the reset countdown;
- a refresh counter (6) connected to refresh input (11) of the reset counter (3) having a refresh input (9), and designed to:

- launch a refresh countdown on each receipt of a refresh command on its refresh input (9);
- only to apply a refresh command to refresh input (11) of the reset counter if the refresh countdown has expired at the time of receipt of the refresh command.

14. Watchdog timer according to either of claims 12 or 13, characterized in that the reset counter (3) has several bits and in that the high-order bit (6) is connected to the reset output.

15. Watchdog timer according to claim 14, characterized in that the counter is included in a register.

16. Watchdog timer according to any of claims 12 to 15, characterized in that it also comprises a logic ET port, an activation input (13) having a logic link with an input of port ET, and in that the reset output has a logic link with another input of port ET.

17. Watchdog timer according to claims 15 and 16, characterized in that the activation input is connected to a register activation bit, and in that the activation bit of the register is connected to the input of logic port ET.

18. Watchdog timer according to any of claims 12 to 17, characterized in that it also comprises:

- a timer input (14)

- a frequency divider (5) equipped with an input connected to timer input (14) and with an output connected to the bits of reset counter (3), so as to decrement the reset counter when a signal is applied by frequency divider (5).

19. Watchdog timer according to any of claims 12 to 18, characterized in that the duration of the refresh countdown is less than the time period separating two decrements of the reset counter.

20. Watchdog timer according to either of claims 18 or 19, characterized in that the refresh counter has several bits (C0-C7) and is connected to the timer input, so as to decrement the reset counter when the clock signal is applied.

21. Watchdog timer according to any of claims 12 to 20, characterized in that the duration of the reset countdown (3) is programmable.